Remarks

The present response is to the Office Action mailed the above-referenced case on June 12, 2008, made final. Claims 1-11, 13-25, 27 and 28 are standing for examination.

Response to Arguments

Applicant's arguments filed 3/10/2008 have been fully considered but they are not persuasive. Applicant's arguments are summarized as:

a. Prior art of record does not disclose an on-chip oscillator.

b. Prior art of record does not disclose that both communication interfaces share a single I/0 terminal.

2. Regarding argument 'a', examiner notes that applicant argues that the oscillator being "on the card does not necessarily mean "on-chip". However, teachings of Atsmon are directed to a smartcard or as applicant described "a pocket sized card with embedded integrated circuits which can process information". The oscillator, known in the art as a device that regulates the processor's computing cycles, is clearly part of the "embedded integrated circuit", and therefore on-chip. The "card" portion of the smartcard is just the protective outer surface without any active functionality. Assuming that the oscillator is on the card but not part of the integrated circuit (in other words, not imprinted on the silicon chip) is completely erroneous.

Applicant's response

After further consideration of the art of Atsmon applicant points out that Atsmon fails to teach an oscillator included on the card, on-chip, or off-chip. The Examiner refers to column 13, lines 4-11 to teach said oscillator. Applicant reproduces said reference below:

> rounding circuitry. The processor is a PIC 16F84, which is fast and contains on-chip data EEPROM. The PIC 16F84 also provides for three options to provide the clock source—(1) external crystal oscillator, (2) external oscillator circuit, and (3) external RC circuit. Because of the size constraint of the electronic card, a crystal clock source could not be used. Also, an external oscillator circuit, while feasible, contains too many components. Accordingly, an RC circuit (R2 and C2) is provided at the OSC1/CLKIN input. With the particular values shown in FIG. 7, the clock frequency selected is 4 MHz. Reset is provided at the MCLR input.

3.

Applicant argues that clearly the above portion of Atsmon teaches that the EEPROM is on-chip and the choice of using an oscillator is an external oscillator, clearly interpreted by anyone with skill in the art as external to the chip, when interpreted in context. Further, the passage states that although an external oscillator is a choice for providing the clock source, it is elected to not be part of the system because both selections (1) and (2) contains too many components to fit in the card. Selection (3) is implemented which is an external RC circuit. Therefore, and without a doubt Atsmon does not teach an on-chip oscillator. Applicant's arguments are not erroneous, as espoused by the Examiner. It is possible to have an external oscillator as specifically taught in Atsmon, which is analogous art.

Further, applicant's invention teaches a modem interface for a one wire modem, the modem interface carries out the FSK (Frequency Shift Keying) and PSK (Phase Shift Keying) modulations, which are reliable and easy to implement on the host, even though other modulations can be chosen. The data is first encoded using the Manchester or Miller code creating transitions even if the data doesn't change. The modulation and demodulation are controlled by the on-chip oscillator (page 4, lines 22-26). Applicant points out that Atsmon teaches communication implementing acoustic waves which require transducers (col. 13, lines 26-28 and col. 25, lines 29-50). Therefore, there is no need in Atsmon for an on-chip oscillator, as claimed.

The Examiner continues

Regarding argument 'b', applicant argues that it is merely shown in the figure of the prior art that there's a single arrow, which can be more than a "single I/0 terminal providing a single connection port" between the processor 169 and interface 190 of the prior art. Examiner notes that prior art teaches that the communication interface is "responsible for detecting information that is formatted according to a particular protocol and converting the information to a format suitable for presentation to processor 169". It is clear that if the interface 190 converts the various protocols shown in figure 13 to "a format" suitable for the processor, there only needs to be a single I/0 terminal from the interface 190 to the processor, shown by the singular arrow in figure 13. Assuming there's more than one connection between the processor 169 and interface 190 contradicts the purpose of having the interface in the first place, as the various protocol ports can just be directed connected to the processor without converting them to "a format" suitable for the processor.

Applicant's response

Applicant clearly claims, "characterized in that both communication interfaces are bidirectional and share a single I/0 terminal providing a single connection port on the secure memory device for both of the communication interfaces." Applicant argues that the single communication interface 190 of Leydier is just that, a single communication interface capable of communicating with processor 169 in a manner that is not disclosed in the art of Leydier. Applicant points out that the Examiner may not assume the hardware implementation of said connection between processor 169 and the connector interface 190. If the Examiner relies upon the processor 169 to represent applicant's secure memory device, the Examiner has presented one communication interface connected to a processor. Applicant argues that the connection interface 190 is an additional device unto itself not needed in applicant's invention and serves to provide three I/O ports for ISO 195, USB 197 and wireless 199 on one side and an undisclosed connection to a processor on the other side. Therefore, Connection interface 190 cannot

read on, nor would one with skill in the interpret as a single I/O terminal *on a secure memory device* providing a single connection port for two incoming communication interfaces, as claimed. **Leydier provides three ports for three different protocol communications, not one port, as claimed.**

Applicant points out the teaching of Leydier clearly states that a connection interface 190 detects information according to a particular protocol and formats it to a form acceptable by the processor. The Examiner states, "is clear that if the interface 190 converts the various protocols shown in figure 13 to "a format" suitable for the processor, there only needs to be a single I/O terminal from the interface 190 to the processor, shown by the singular arrow in figure 13. Assuming there's more than one connection between the processor 169 and interface 190 contradicts the purpose of having the interface in the first place, as the various protocol ports can just be directed connected to the processor without converting them to "a format" suitable for the processor." Applicant argues that said statement by the Examiner is pure conjecture and not part of the teaching of Leydier. The purpose of the interface is clearly to convert protocol formats, as recited in Leydier. The Examiner's assumption that the interface is to provide a single I/O port to the processor, is just that, an assumption. Said Leydier teaching does not recite, nor would one with skill in the art assume the teaching is interpreted as, "detects information according to a particular protocol from a plurality of protocols wherein all protocols are formatted into a single format acceptable to the processor", which would be the only basis for the Examiner making the assumption that the interface 190 provides a single I/O terminal and port to the processor.

Applicant believes claims 1 and 15 are patentable over the art of Atsmon and Leydier as applicant has effectively responded to the Examiner's Response to Arguments portion of the present Office Action. For the reasons given herein and in the previous response, the Examiner has not proven a valid prima facie case of obviousness against applicant's invention as claimed.

Dependent claims 2-11, 13-14, 16-25, and 27-28 are patentable on their own merits, or at least as dependent upon a patentable base claim.

Summary

As all of the claims standing for examination have been shown to be patentable over the art of record, applicant respectfully requests reconsideration, and that the present case be passed quickly to issue. If there are any time extensions needed beyond any extension specifically requested with this response, such extension of time is hereby requested. If there are any fees due beyond any fees paid with this amendment, authorization is given to deduct such fees from deposit account 50-0534.

Respectfully Submitted,
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